Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer to the claimed and/or disclosed subject matter, and the applicant and/or assignee reserves the right to claim this subject matter and/or other disclosed subject matter in a continuing application.

Listing of Claims:

1. (Previously presented): An apparatus comprising:

an individual memory device including a memory array having a first portion and a second portion, the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor and the second portion of the memory array is accessible only by a second processor, wherein the memory array further comprises a third portion that is different than the first portion and the second portion, the third portion of the memory array accessible by both the first processor and the second processor, and wherein the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.

Claim 2 (Cancelled)

3. (Original): The apparatus of claim 1, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal.

4. (Original): The apparatus of claim 3, wherein the first portion and the second portion of the memory array are coupled to a same power supply potential.

Claim 5 (Cancelled)

6. (Previously presented): The apparatus of claim 1, wherein the memory array is further adapted to increase the size of the first portion and decrease the size of the second portion due to an increase in the operational load of the first processor.

7. (Original): The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array substantially simultaneously as the second processor accesses the second portion of the memory array.

8. (Original): The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may read the first portion of the memory array as the second processor writes to the second portion of the memory array.

9. (Original): The apparatus of claim 1, wherein the memory array comprises memory selected from the group consisting of static random access memory, dynamic random access

memory, read only memory, electrically erasable and programmable read only memory, and flash memory.

Claims 10-34 (Canceled)